EXAMINER'S AMENDMENT

Applicant(s): Dagnachew Birru
Serial No.: 09/812,437
Filed: March 20, 2001
For: A LOW-COST HIGH-SPEED MULTIPLIER/ACCUMULATOR UNIT FOR DECISION FEEDBACK EQUALIZERS
Art Unit: 2637
Examiner: Goshtasbi, Jamsid

Attorney Docket No.: US010069

IN THE CLAIMS:

Please consider the following claims:

1. (currently amended) In a feedback equalizer device implementing a filter unit performing convolution operations between filter coefficients and one of a plurality of first discrete digital level values for generating a filter output, a multiplier device for multiplying a first discrete digital level value with a filter coefficient for said convolution operation, said multiplier device comprising:

a decoder device for receiving and decoding an encoded, first discrete digital level value to be multiplied with a filter coefficient, and implementing logic for generating control signals according to said first digital level value;

a first sub-multiplication circuit receiving said filter coefficient and implementing logic for multiplying said filter coefficient by ~~a positive value,~~ a negative value ~~or zero (0)~~ in accordance with a first set of control signals and generating a first intermediate multiplication result therefrom;

12 a second sub-multiplication circuit ~~simultaneously~~ receiving said first intermediate multiplication result and implementing logic for multiplying said first intermediate result ~~filter coefficient~~ by a positive value, ~~a negative value~~ or zero (0) in accordance with a second set of control signals and generating a second intermediate result therefrom;

a third sub-multiplication circuit for shifting bits to effect a multiplication of one of said first or second intermediate result with a discrete digital value different than any of said first plurality of discrete digital level values, and generating a third intermediate result; and